CLAIMS

What is claimed is:

1. A clock divider reset circuit, comprising:

a first inverter coupled to a counter;

a first buffer coupled to the first inverter,

a comparator coupled to an output of the counter;

an OR gate coupled to an output of the comparator;

a second buffer coupled to the OR gate and the first buffer; and

a feedback path coupling the output of the comparator to the counter.

2. The circuit of claim 1, wherein the first inverter is coupled to a reset input of the counter.

3. The circuit of claim 2, wherein the reset input comprises an active high reset input.

4. The circuit of claim 1, wherein a clock input of the counter is coupled to an external pin clock signal.

5. The circuit of claim 1, wherein a clock input of the counter is coupled to a PLL.

6. The circuit of claim 1, wherein a first input of the comparator is coupled to a count output of the counter.

7. The circuit of claim 1, wherein a second input of the comparator is coupled to a plurality of signals associated with a full count value.

8. The circuit of claim 1, wherein the output of the second buffer is a reset signal.

9. The circuit of claim 1, wherein the output of the OR gate is a clock divider reset signal.

10. The circuit of claim 1, wherein the feedback path comprises a second inverter coupled to an output of the comparator and an input of the counter.

11. The circuit of claim 10, wherein the second inverter is coupled to a count enable input of the counter.

12. The circuit of claim 1, wherein an output of the first buffer is coupled to an input of the OR gate.

13. The circuit of claim 1, wherein the first buffer is coupled to an external reset signal.

14. The circuit of claim 13, wherein the external reset signal comprises an active low reset signal.

15. A clock divider reset circuit, comprising:

a first inverter coupled to a counter;

a second inverter coupled to the first inverter,

a comparator coupled to an output of the counter;

a NOR gate coupled to an output of the comparator;

a third inverter coupled to the NOR gate and the second inverter; and

a feedback path coupling the output of the comparator to the counter.

16. The circuit of claim 15, wherein the first inverter is coupled to a reset input of the counter.

17. The circuit of claim 16, wherein the reset input comprises an active high reset input.

18. The circuit of claim 15, wherein the output of the NOR gate is a clock divider reset signal.

19. The circuit of claim 15, wherein the feedback path comprises a fourth inverter coupled to an output of the comparator and an input of the counter.

20. The circuit of claim 15, wherein an output of the second inverter is coupled to an input of the NOR gate.

21. A method for resetting a chip or a circuit, comprising:

generating a limited duration clock divider reset, wherein the limited duration clock divider reset is independent from a reset signal used to reset the chip or the circuit; and

resetting the chip or the circuit using the generated limited duration clock divider reset.

22. A method for resetting a chip or a circuit, comprising:

buffering a main reset input signal;

inverting the main reset input signal to create an active high reset signal;

resetting a counter utilizing the active high reset signal;

comparing a counter output value and a counter-associated value in a comparator to obtain a comparator output value; and

applying an OR logical operation to the comparator output.

23. The method of claim 22, further comprising generating a limited duration clock divider reset from the output of the OR logical operation.

24. The method of claim 22, further comprising applying the OR logical operation to the buffered main reset input signal.

25. The method of claim 22, further comprising inverting the comparator output.

26. The method of claim 25, further comprising enabling the counter via the inverted comparator output.

27. The method of claim 22, further comprising receiving an external pin clock signal by a clock input of the counter.

28. The method of claim 22, further comprising receiving a PLL by a clock input of the counter.

29. The method of claim 22, further comprising receiving a full count value signal by an input of the comparator.

30. The method of claim 29, wherein an output of the full count value is based on a maximum count value of the counter.